AMENDMENTS TO THE CLAIMS

1.(original) A method of connecting SONET/SDH termination devices with payload processing devices, comprising:

(a) providing a transmit interface operative to receive incoming SONET/SDH signal streams and convert said SONET/SDH signal streams into outgoing low voltage differential signal (LVDS) levels with said SONET/SDH signal streams mapped into 8B/10B control characters so as to label SONET/SDH frame boundaries; and

(b) providing a receive interface operative to receive incoming LVDS signal levels and convert said LVDS signal levels into outgoing SONET/SDH signal streams with decoding of said 8B/10B control characters labeling SONET/SDH frame boundaries into SONET/SDH control signals.

2.(original) A method according to claim 1, wherein said SONET/SDH frame boundaries include transport frame, high-order path frame and low-order path frame boundaries.

3.(original) A method according to claim 1, including mapping a descrambled SONET/SDH data stream into 8B/10B control characters of to ensure data transitions on serial links and to preserve DC balance.

4.(original) A method according to claim 1, including treating positive and negative disparity codes of said 8B/10B control characters having an even number of ones and zeros as separate control characters.

5.(currently amended) A method according to claim 1, including storing single bytes for N distinct streams within a SONET OC-N/SDH stream ~~signals~~ in a buffer and transferring said single bytes signals using a universal frame pulse with a software programmable delay to allow transfer of one or more SONET/SDH signals over multiple links.

6.(original) A method according to claim 1, including providing transparent in-band error reporting where errors detected at a SONET/SDH receiver can be transferred to a transmitter to construct remote error and defect indication codes.

7.(original) A method according to claim 1, including inserting a pseudo-random bit sequence pattern in serial transmit links to allow data path verification prior to injection of actual payload.

8.(currently amended) A method according to claim 1, including monitoring pseudo-random bit sequence patterns including said inserted pseudo-random bit sequence pattern ~~using line code violations of 8B/10B characters to monitor error performance of serial links~~.

9.(currently amended) A method according to claim 1, including overwriting a first unused SONET/SDH byte ~~one of the E1 and B1 bytes~~ to form a pattern which allows in-service monitoring of link functionality as well as monitoring of downstream cross-connect mis-configurations.

10.(currently amended) A method according to claim 9, wherein a second unused SONET/SDH overhead byte is ~~bytes in E1 are~~ overwritten with a complement of a value in ~~B1 bytes~~ said first unused byte.

11.(original) A bus interface device for connecting SONET/SDH termination devices with payload processing

devices, comprising:

(a) a transmit interface operative to receive incoming SONET/SDH signal streams and convert said SONET/SDH signal streams into outgoing low voltage differential signal (LVDS) levels with said SONET/SDH signal streams mapped into 8B/10B control characters so as to label SONET/SDH frame boundaries; and

(b) a receive interface operative to receive incoming LVDS signal levels and convert said LVDS signal levels into outgoing SONET/SDH signal streams with decoding of said 8B/10B control characters labeling SONET/SDH frame boundaries into SONET/SDH control signals.

12.(original) A bus interface device according to claim 11, wherein said SONET/SDH frame boundaries include transport frame, high-order path frame and low-order path frame boundaries.

13.(original) A bus interface device according to claim 11, including a plurality of 8B/10B encoder blocks operative to map a descrambled SONET/SDH data stream into 8B/10B control characters of to ensure data transitions on

serial links and to preserve DC balance.

14.(original) A bus interface device according to claim 11, including a buffer for storing signals, wherein said signals are transferred using a universal frame pulse with a software programmable delay in order to allow transfer of one or more SONET/SDH signals over multiple links.

15.(original) A bus interface device according to claim 11, including a pseudo-random bit sequence pattern in serial transmit links to allow data path verification prior to injection of actual payload.

16.(original) A bus interface device according to claim 11, including a character alignment block and a frame alignment block operative to detect line code violations of 8B/10B characters in order to monitor error performance of serial links.

17.(currently amended) A bus interface device according to claim 11, including a pseudo-random bit sequence generator detector operative to monitor and overwrite E1 and B1 bytes to form a pattern which allows in-service monitoring of link functionality as well as monitoring of

downstream cross-connect mis-configurations in serial transmit links operative to allow data path verification prior to injection of actual payload.

18.(original) A bus interface device according to claim 17, wherein bytes in E1 are overwritten with a complement of a value in B1 bytes.

19.(new) A method according to claim 1, including overwriting a first unused SONET/SDH byte to form a pattern which allows in-service monitoring of link functionality as well as monitoring of downstream cross-connect mis-configurations.

20.(new) A method according to claim 9, wherein a second unused SONET/SDH overhead byte is overwritten with a complement of a value in said first unused byte.